a third semiconductor layer of said second conductivity type higher in an impurity concentration and thinner than said second semiconductor layer, and provided on a surface of said second semiconductor layer;

a fourth semiconductor layer of said first conductivity type provided on a surface of said third semiconductor layer;

a fifth semiconductor layer of the second conductivity type selectively provided in a surface of said fourth semiconductor layer and opposing said third semiconductor layer through said fourth semiconductor layer;

a first main electrode disposed across and connected with surfaces of said fourth and fifth semiconductor layers;

a second main electrode provided on said second main surface of said first semiconductor layer;

an insulating film provided on a portion of said fourth semiconductor layer interposed between said third and fifth semiconductor layers; and

a control electrode facing said portion through said insulating film so that said portion forms a channel region.

23. (New) The insulated gate semiconductor device according to claim 22, wherein said second semiconductor layer extends through said first semiconductor layer and is partially exposed in said second main surface of said first semiconductor layer.

24. (New) The insulated gate semiconductor device according to claim 22, further comprising a sixth semiconductor layer of said second conductivity type higher in an impurity concentration than said second semiconductor layer provided between said first and second semiconductor layers.

25. (New) The insulated gate semiconductor device according to claim 24, wherein said sixth semiconductor layer extends through said first semiconductor layer and is partially exposed in said second main surface of said first semiconductor layer.

26. (New) The insulated gate semiconductor device according to claim 22, wherein said first main electrode is not contacting any other semiconductor layer than said fourth and fifth semiconductor layers.

27. (New) A method of manufacturing an insulated gate semiconductor device, comprising the steps of:

(a) forming a semiconductor substrate defining first and second main surfaces and having a first semiconductor layer of a first conductivity type and a second semiconductor layer of a second conductivity type, said first semiconductor layer being exposed in said first main surface and said second semiconductor layer being exposed in said second main surface;

(b) implanting and diffusing impurity of said second conductivity type to an impurity concentration higher than an impurity concentration of said second semiconductor layer into said second main surface of said semiconductor substrate to form a third semiconductor layer of said second conductivity type in a surface portion of said second semiconductor layer;

(c) implanting and diffusing impurity of said first conductivity type in a surface of said third semiconductor layer to form a fourth semiconductor layer of said first conductivity type in a surface portion of said third semiconductor layer, wherein said third semiconductor layer is so formed as to be thinner after forming said fourth semiconductor layer than said second semiconductor layer remaining;

(d) selectively implanting and diffusing impurity of said second conductivity type in a surface of said fourth semiconductor layer to selectively form a fifth semiconductor layer of said second conductivity type in a surface portion of said fourth semiconductor layer;

(e) forming an insulating film on surfaces of said fourth and fifth semiconductor layers;

(f) providing a conductor on said insulating film;

(g) selectively removing said conductor to form a control electrode facing a portion of said fourth semiconductor layer interposed between said third and fifth semiconductor layers through said insulating film so that said portion forms a channel region;

(h) providing an insulating layer on said surface of said insulating film and an surface of said control electrode;

(i) selectively removing said insulating layer and said insulating film in a region that lies across said surfaces of said fourth and fifth semiconductor layers;

(j) providing a conductor disposed across said surfaces of said fourth and fifth semiconductor layers exposed after said step (i) to form a first main electrode; and

(k) providing a conductor on said first main surface of said semiconductor substrate to form a second main electrode.

28. (New) The method of manufacturing the insulated gate semiconductor device according to claim 27 wherein said step (a) comprises the steps of:

(a-1) preparing a semiconductor substrate body of the first conductivity type having two main surfaces; and

(a-2) providing a semiconductor layer of said second conductivity type with a low impurity concentration by the epitaxial growth on one of said main surfaces of said semiconductor substrate body to form said second semiconductor layer.

29. (New) The method of manufacturing the insulated gate semiconductor device according to claim 27, wherein said step (a) comprises the steps of:

(a-1) preparing a semiconductor substrate body of said second conductivity type with a low impurity concentration having two main surfaces;

(a-2) implanting impurity of said first conductivity type into one of said main surfaces of said semiconductor substrate body; and

(a-3) diffusing said impurity implanted into said one main surface to form said first semiconductor layer of said first conductivity type.

30. (New) The method of manufacturing the insulated gate semiconductor device according to claim 29, wherein said step (a-2) comprises the step of (a-2-1) selectively implanting impurity of said first conductivity type into said one main surface of said semiconductor substrate body.

31. (New) The method of manufacturing the insulated gate semiconductor device according to claim 27, wherein said semiconductor substrate formed in said step (a) further comprises a sixth semiconductor layer of said second conductivity type with a high impurity concentration interposed between said first semiconductor layer and said second semiconductor layer.

32 . (New) The method of manufacturing the insulated gate semiconductor device according to claim 31, wherein said step (a) comprises the steps of:

(a-1) preparing a semiconductor substrate body of said first conductivity type having two main surfaces; and

(a-2) sequentially forming said sixth semiconductor layer and said second semiconductor layer by the epitaxial growth on one of said main surfaces of said semiconductor substrate body.

33. (New) The method of manufacturing the insulated gate semiconductor device according to claim 31, wherein said substrate forming step (a) comprises the steps of:

(a-1) preparing a semiconductor substrate body of said second conductivity type with a low impurity concentration having two main surfaces;

(a-2) forming said sixth semiconductor layer by implanting impurity of said second conductivity type and then diffusing on one of said main surfaces of said semiconductor substrate body; and

(a-3) implanting and then diffusing impurity of said first conductivity type in a surface of said sixth semiconductor layer to form said first semiconductor layer.

34. (New) The method of manufacturing the insulated gate semiconductor device according to claim 33, wherein said step (a-3) comprises the steps of:

(a-3-1) selectively implanting impurity of said first conductivity type into the surface of said sixth semiconductor layer; and

(a-3-2) diffusing said impurity selectively implanted into the surface of said sixth semiconductor layer.

35. (New) The method of manufacturing the insulated gate semiconductor device according to claim 27, wherein, if the impurity concentrations in said second semiconductor layer, said third semiconductor layer and said fourth semiconductor layer are taken as C2, C3, C4, respectively, said steps (b) and (c) are carried out so that the following relation is satisfied:

$C2<C3<C4$.

36. (New) The method of manufacturing the insulated gate semiconductor device according to claim 27, wherein said step (d) comprise the steps of:

(d-1) forming a resist pattern selectively having an opening in a surface of said fourth semiconductor layer on said surface of said fourth semiconductor layer; and

(d-2) implanting and diffusing impurity of said second conductivity type using said resist pattern as a mask to selectively form a fifth semiconductor layer of said second conductivity type in a surface portion of said fourth semiconductor layer.

37. (New) The method of manufacturing the insulated gate semiconductor device according to claim 27, wherein said step (i) comprises the steps of:

(i-1) forming a resist pattern selectively having an opening that lies across said surfaces of said fourth and fifth semiconductor layers on said surface of said insulating layer; and (i-2) selectively removing said insulating layer and said insulating film using said resist pattern as a mask.

38. (New) The method of manufacturing the insulated gate semiconductor device according to claim 30, wherein said step (a-2) further comprises the step of (a-2-2) forming a resist pattern having a selectively formed opening on said one main surface of said semiconductor substrate body; and

said step (a-2-1) comprises the step of (a-2-1-1) selectively implanting impurity of said first conductivity type into said one main surface of said semiconductor substrate body using said resist pattern formed on said one main surface as a mask.

39. (New) The method of manufacturing the insulated gate semiconductor device according to claim 34, wherein said step (a-3) further comprises the step of (a-3-3) forming a resist pattern having a selectively formed opening on the surface of said sixth semiconductor layer; and

said step (a-3-1) comprises the step of (a-3-1-1) selectively implanting impurity of said first conductivity type into the surface of said sixth semiconductor layer using said resist pattern formed on the surface of said sixth semiconductor layer as a mask.--